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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,734	12/22/2000	Colin Davidson	0325.00436	4619

21363 7590 07/17/2002

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EXAMINER

SUNDARAM, T R

ART UNIT PAPER NUMBER

2858

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/747,734

Applicant(s)

Colin Davidson et al.

Examiner

T. R. Sundaram

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Feb 27, 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on Feb 27, 2001 is/are a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- *See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 6) ☐ Other:

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DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required if and when the application is allowed.
2. The drawings are objected to because, in Fig.1, the lower abscissa does not have a scale. The "10" that is indicated along the bottom right is said to be "region" (page 1, line 14 of specification), so that it is quite unclear what one nanosecond is supposed to represent along this scale.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract is objected to in terms of content and length. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. The form and legal phraseology often used in patent claims, such as "**comprising**," should be avoided. The abstract should describe the

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disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ahmad et al.*, in view of *Gascoyne* and *Agarwal et al.*

Regarding claim 1, *Ahmad et al.* discloses an integrated circuit (13, Fig. 1 and Fig. 2) comprising: a test circuit (upper half, Fig. 2; and column 3, lines 62-63) configured to generate a test signal (53, Fig. 2; and column 6, lines 14 ff) and can be used to predict failure of said integrated circuit (column 1, lines 16-17; column 2, lines 63-67; column 4, line 29).

Ahmad et al. does not expressly disclose a test signal having a predetermined pulse width in response to a control input, wherein said test signal tracks process corners and which can be used to predict failure of said integrated circuit, albeit it discloses (Figs. 8-10) various methods for performing the self test on the built-in circuits.

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Gascoyne discloses a process monitoring circuit (Fig. 3) for integrated circuits and enabling the test mode (column 5, lines 11-14) using pulse width (column 6, lines 32 ff) of the signal. *Gascoyne* also discloses tracking the process corners (Fig. 6; and column 6, line 54 to column 7, line 6)

Agarwal et al. discloses an integrated circuit with embedded SRAM memory blocks (Figs. 3B and 8); specifically, it discloses using pulse width for providing timing for address-capture and output-data capture (column 34, lines 25 ff).

Ahmad et al., *Gascoyne* and *Agarwal et al.* and the present invention are analogous art because they all deal with semiconductor devices in general and with testing of memory blocks in particular. *In re Deminski*, 796 F.2d 436, 442, 230 USPQ 313, 315 (Fed. Cir. 1986); *In re Wood*, 599 F.2d 1032, 1036, 202 USPQ 171, 174 (CCPA 1979).

A person of ordinary skill in this art would be familiar with prior art techniques for testing of semiconductor devices in general and techniques for providing controlled test inputs in particular.

Therefore, at the time of the invention, it would have been obvious for a person of ordinary skill in the art to have combined the teachings of *Ahmad et al.*, *Gascoyne* and *Agarwal et al.*, and to have arrived at the invention of claim 1.

The Suggestion/Motivation for doing so would have been that built-in self-test (BIST) circuits are more the norm than an exception in most modern integrated circuit architecture, including in SRAMs. *Ahmad et al.* teaches a specific type of such a circuit, while *Gascoyne* and

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Agarwal et al. teach various variations for test signal input and control. Combining the different techniques is a matter of engineering design choice.

Therefore, claim 1 is obvious and unpatentable over *Ahmad et al.*, *Gascoyne* and *Agarwal et al.*

Regarding claim 2, *Ahmad et al.* discloses that the control input (53, Fig. 2) comprises a write enable input (Fig. 8; and column 9, lines 26 ff).

Regarding claim 3, *Ahmad et al.* discloses a transition to a write enable input (column 9, lines 39-45).

Regarding claim 4, *Ahmad et al.* discloses using transition from HIGH to LOW logic levels (column 3, lines 1-15).

Regarding claims 5-7, *Agarwal et al.* discloses that the configurable logic blocks may be user definable (column 2, line 59 ff) and that pulse width can also be user controlled (column 34, lines 25 ff; and column 40, lines 34-36). Also, *Ahmad et al.* discloses that the configuration is fuse programmable (column 10, lines 25 ff).

Regarding claim 8, *Ahmad et al.* discloses that the configuration inputs are determined by a metal masking step during fabrication (column 3, lines 39-51).

Regarding claim 9, *Ahmad et al.* discloses that the technique can be used to test static random access memory (SRAM) cells (column 7, lines 44-48).

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Regarding claim 10, *Ahmad et al.* discloses that the test circuit is configured to predict failure of one or more cells (Figs. 3-5; column 4, lines 23-32; and column 9, line 58 to column 10, line 10).

Regarding claim 11, although this independent apparatus claim uses the means-plus-function format of 35 U.S.C. 112, Sixth Paragraph, all the structural limitations (including those recited in the specification) are disclosed by *Ahmad et al.*, *Gascoyne* and *Agarwal et al.* Therefore, claim 11 is also obvious and unpatentable over *Ahmad et al.*, *Gascoyne* and *Agarwal et al.*

Regarding method claims 12-15 these method claims recite the same limitations as in the apparatus claims already considered, and are the represent the obvious manner in which the circuit would be utilized. Therefore, claims 12-15 are also obvious and unpatentable over *Ahmad et al.*, *Gascoyne* and *Agarwal et al.*

Regarding claim 16, *Ahmad et al.* discloses life testing (abstract).

Regarding claim 17, *Ahmad et al.* discloses a sorting step following the testing (column 10, lines 23 ff).

Regarding claim 18, *Ahmad et al.* discloses repairing faulty integrated circuits (column 2, line 39).

Regarding claim 19, burn-in failures occur mainly due to poor contacts.

Regarding claim 20, *Ahmad et al.* discloses voltage control of the tests (column 3, lines 1-15).

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Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

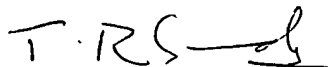
Krug discloses a test arrangement in which test circuits are provided on the wafer.

Restoker et al. discloses a method for testing individual unsingulated die on a wafer.

Farnworth et al. discloses a reduced terminal test system.

Fuller et al. discloses a remote test module for test equipment.

7. Any inquiry concerning this communication should be directed to Dr. T. R. (Joe) Sundaram at telephone number (703) 308-6821. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, N. Le can be reached at (703) 308-0750.



T. R. Sundaram

July 12, 2002